



## Renaissance FAEs

Our Once and Future Saviors

by Kevin Morris, FPGA and Structured ASIC Journal

In classical music, they are the organists.

My brother, an accomplished professional trumpet player, had just completed a performance for solo piccolo trumpet and organ. I was looking at his immaculately maintained instrument and noticed that one of the tuning slides was so light, it seemed it could just fall off the horn if the performer held it at the wrong angle.

"What would you do if this fell off during a performance?" I asked.

Seemingly without thinking, he replied "Oh, the organist would catch it and replace it."

I was briefly puzzled.

"Yes," he continued, "She'd catch it and put it back – tuned exactly right - while simultaneously sight-reading five lines of music at different tempos and in different keys, playing with both hands and both feet, painting her nails... and playing jacks to keep herself from getting bored."

In the world of FPGAs, they are FAEs.

It starts innocently enough. Let's say your next project is to design a third-order, exponentially-damped, semi-dihedral Frak-band demodulator. You've thought about using an FPGA. However, although you're one of the industry's leading authorities on Frak-band demodulation, you're not too good with VHDL.

One day, however, you're at a trade show and you succumb to the siren song of the development kit. Sitting there on the table – professionally lit with high-intensity halogen display fixtures -- sits the "Frak-band demodulator FPGA development kit." You stare, blink your eyes a couple of times (trade shows have been known to cause minor hallucinations), and step up for the

demo. There, inside a box, all glossy-printed like it was meant to be on sale at Wal-Mart, is an FPGA development board pre-designed with those hard-to-find, proprietary, FrakNC17 connectors, the requisite USB cable, free design software, and a CD with a working Frak-band demodulator reference design and IP library.

Of course, this is only ALMOST too good to be true. The reference design is only a second-order F-b demod, and it's linearly damped, but you certainly have the Frak-cred to kick it up to industrial standards. Down goes the company AmEx, and with a transaction smaller than the business lunch you just bought, you're on your way to Frak-band nirvana.

Well, almost.

Let's fast-forward about two months.

You see, a third-order FBD takes quite a bit more hardware than the simple reference design, and you had to upgrade to a dev board with a much larger FPGA. Next, you had to get your own daughterboard built with the requisite connectors. The "free" design tools that came with the kit tapped-out on just the front-end of your design, so your company had to spring for the full-boat expensive stuff. You spent a week in tool training class and now your design is kinda' stitched together, but every time you run synthesis you get back volumes of timing violations. You also keep running into issues with the number of available clock domains in the area of the FPGA with the I/O and memory resources you need, and your attempt at floorplanning just made things worse. Your boss is reminding you that your project has fallen six months behind in only two months time and he hasn't yet noticed that it is also now (by your private estimate) 120X over budget.

Annual performance reviews start in one month.

Layoffs are rumored.

It's time to call your FAE.

Like the superhero organists of old, he blows through the door sporting his Metallica T-shirt and carrying a laptop under his arm. He grabs a copy of your design. His fingers fly across the keyboard. Special diagnostic tools and scripts emerge from the Ether. New settings and parameters drive the design tools down unfamiliar paths. Your dihedral expansion module is replaced with a barrel-shifter multiplexed to a hard-wired 18-bit multiplier unit, and somehow

that pushes  $F_{max}$  up by 40%. He simultaneously discovers and rectifies a race condition you'd never even noticed in your design. Time seems to stand still...

A day later, your development board is quietly demodulating not just one, but two parallel Frak-band streams, and doing it at a bit-error rate lower than anything seen in the industry. Power consumption is only half of what you'd allotted, and it looks like you'll be able to replace those expensive connectors with two paperclips and a thumbtack thanks to the automatic equalization circuit the FAE added to your incoming FB lines.

The FAE's chair is empty and only his crinkled business card remains. He is off to save another project.

Even the venerable FAE is facing a challenge these days, however. His Kryptonite? The expanded diversity of FPGA applications. In the past, an FAE could spend the few-months' effort to become a black-belt ninja in simulation, synthesis, and place-and-route, and then leave the nest to begin saving the world.

Today, however, he needs to be able to help embedded designers, so he also needs to know about busses, processor configuration, embedded debuggers, real-time operating systems, and firmware. If the customer is doing DSP, it pays know some linear algebra, be pretty adept with MATLAB and Simulink, and understand how to tap out a fast FIR filter without looking like a hack. When high-speed serial data is involved, he needs to not only know some signal integrity lingo, but also how to use the special FAE-only eye-diagram stretcher-calipers available with secret settings on programmable pre-emphasis.

It's scary.

The amount of specialized, domain-specific training and expertise required to become an effective FAE in today's FPGA world is staggering. Many long-time FAEs are starting to feel like TV-show doctors, walking in the room exuding confidence while spouting off jargon-laden phrases on which they have only the narrowest conceptual grasp. "So, you're saying that we're doing a Hough transform after edge detection on the incoming stream from the satellite, and fields with crop-circles are detected reliably as long as the  $m$  and  $b$  parameters are properly quantized in the FPGA's ... What?"

The next day, they're off with a different customer looking at H.264 decompression.

FAEs are the quiet heroes behind the success of the FPGA industry. They bridge the sometimes enormous gap between the documentation and guidance provided in the dev kits and app notes and what is required to get a real, working, production-quality FPGA designs out the door. Without these silent warriors, untold multitudes of design projects would have failed and, with that, the credibility of FPGAs as design solutions irreparably damaged.

As FPGAs move into new and more demanding markets, these re-invented FAEs face a serious challenge in amassing the expertise they need to save us all from our own ignorance. Next time your FAE visits, take a minute to thank him or her, and try to imagine how hard it is to continue wearing the cape in this age of complexity and skepticism.

Long live the FAE!

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