



Express Yourself

The Ins and Outs of PCI Express

“When I was your age, I walked 10 miles to school – each way – barefoot in the snow (OK, maybe not).”

“When I was your age, I had something called a record player, and I listened to albums, appreciating a band for more than the one song that got voted onto the top 20 on TRL.”

“When I was your age, I designed my systems using an ISA bus for my I/O interconnect. That’s how it was done. And we LIKED IT.”

It is the job of each new generation to move us forward, sometimes in small steps, sometimes in monstrous leaps. And so it goes for I/O interconnect. In the early 1990s, the first-generation Industry Standard Architecture (ISA) bus was slowly phased out in favor of the more robust Peripheral Component Interconnect (PCI) local bus architecture. PCI is a 64-bit bus, usually implemented as a 32-bit bus, running at clock speeds of 33MHz for a throughput rate of 133MB/sec. Next came PCI-X (meaning PCI-Extended). PCI-X didn’t stray far from PCI, maintaining the established parallel bus structure, but it delivered more performance, with a throughput rate up to 1 GB/sec.

High-speed peripherals like Gigabit Ethernet and USB began pushing the limits of the PCI parallel bus structure, demanding more and more bandwidth. Then along came PCI Express. Although it carries on the PCI name, it actually has very little resemblance to its forefathers. PCI Express has a layered architecture, with a software layer, a transaction layer, a data link layer, and a physical layer. It has abandoned the parallel bus structure for a two-way serial approach that carries data in packets along pairs of point-to-point lines. PCI Express bit rates are 2.5Gb/sec per lane direction, and is scalable up to 16 lanes (you do the math...).

But PCI Express isn’t a total rebel. It maintains backward compatibility with the older PCI bus structures, and core PCI attributes, including the usage

model and software interfaces, are still in place. This means that existing applications and drivers are not changed. Essentially, it's just the BMX-riding, iPod-listening, espresso-drinking, cellphone-carrying, X-Games watching member of the PCI clan – fast, smart, and a little bit complicated to understand at first.

Not Your Average Standard

Of course, a standard of such broad importance needs to be managed. To that end, the PCI-SIG (PCI Special Interest Group) has been in place for many moons now – since 1992 in fact – chartered with the development and management of the PCI bus specification.

With more than 800 member companies, the PCI-SIG plays a very important role in establishing credibility for solutions on the market through the PCI compliance program. The compliance program includes compliance workshops (known as Plugfests), the compliance checklist, and the PCI integrator's list. The PCI integrator's list is the equivalent of The Good Housekeeping Seal of Approval for PCI Express solutions. If you're on the integrator's list, you've successfully completed the Plugfest and the compliance checklist. Long story short, if you want your PCI Express product to be selected by any large company, you'd better be on this list.

To Bridge or Not to Bridge

To determine the extent to which you might include PCI Express in your next design, you need to weigh several factors. First, determine what your product is going to plug into. If it's an existing product, will it continue to connect into the same infrastructure as it did before? If so, you may want to consider a bridging solution (actually a reverse bridging solution) that will allow you to take PCI Express and convert it to PCI or PCI-X for the purpose of plugging into your system board. From a design standpoint, bridging presents less of a challenge, because your PCI Express signals will be traveling a much smaller distance – just over the bridge – and then they'll follow the same path as before. This is a reasonable interim step for you to be able to support PCI Express in your application while keeping your existing infrastructure in place. The downside of this approach, however, is that you'll still be limited by the abilities of the existing PCI or PCI-X. You won't be able to leverage the incremental capabilities of PCI Express.

Then, there's the bold move. Take the plunge. Plug into a PCI Express slot. Just be ready to face the challenge. For ASIC designers, one of the most

significant transition issues facing a first time PCI Express user is the high-speed physical layer, or PHY. PCI Express is based on a 2.5Gb/sec PHY, a high-speed component that introduces the issue of analog into your design. On the upside, you're going to have a lot less to worry about at the system board level because your data should travel more smoothly than it would over the bridge. But your signal will be longer, and you have to work within the constraints of the PCI Express standard.

The PHY is less of an issue for FPGA designers because the programmable logic suppliers have handled it "behind the curtain" for designers with embedded high-speed I/Os.

Click Here for Help

Once you decide to make the move PCI Express, you'll find that there is no shortage of potential partners to help with your FPGA or ASIC design challenge.

On the FPGA front, all of the major suppliers offer PCI Express solutions. Xilinx points out that FPGAs provide a desirable level of flexibility for adopting PCI Express. "PCI Express, when connected to other protocols, is going to have FIFOs and buffering as well as multi-channel memories," said Ron Digiuseppe, IP Marketing at Xilinx. "You could define a structured ASIC to handle that, but the FPGA provides a lot more freedom to define multiple applications." If cost and performance come into the picture, Xilinx says their EasyPath structured ASIC solution presents a solid alternative. In addition, Xilinx supports PCI Express for both their performance-driven Virtex-4 and their low-cost Spartan-3 solutions. "We're really excited about the possibilities for Spartan-3 with PCI Express," said Digiuseppe. "We recently released our IP core for Spartan. For less than \$15, our customers have access to a 90nm chip with PCI Express."

Altera emphasizes ease of use for their PCI Express portfolio. Like Xilinx, they have solutions that address both the low-cost Cyclone II customers and the high-performance Stratix-II and HardCopy customers. "Our intention is to make PCI Express design very simple," said Eugene Ahn, product marketing manager, IP & Technology Marketing at Altera. "To the user, our goal is to make all of the complexity involved in the transition from PCI to PCI Express transparent. It's as simple as answering questions on our drop-down menu to determine what device they would like to use, what PCI Express link, and so on. On the high-density side, we have customers requesting the ability to put several PCI Express links on the Stratix. We can seamlessly migrate this

gigantic Stratix II FPGA to a HardCopy II structured ASIC with no work and dramatically lower the cost of the parts.”

LSI Logic concedes that for a single lane PCI Express implementation, ASICs and FPGAs are both viable choices for designers. However, they say that when performance needs require line rates, low latencies and multiple boards, their RapidChip Platform ASIC can offer a clear performance advantage. “A single lane in PCI Express will give you 2.5Gb/sec throughput in one direction,” said Harmel Sangha, Director, CoreWare Marketing, LSI Logic Corporation. “At any one time data can be flowing in both directions because it’s a full duplex architecture. In order to increase the throughput of the bus, you can have 2, 4, 8, or 16 lanes. So, 8 lanes times 2.5Gb is 20Gb/sec in each direction. That’s where the very high performance comes in. If you want to implement a 4-port switch with low port latency, then your only choice is an ASIC or Platform ASIC.” LSI Logic also offers PCI Express cores from 3rd party IP partners as part of their CoreWare PCI Express portfolio.

EDA vendors also play an important role in enabling the transition to PCI Express for both ASIC and FPGA designers.

Cadence Design Systems has what they call a complete “eco-system” for PCI Express. They offer a PCI Express vertical solution that integrates Cadence soft IP, Rambus hard IP, Denali verification IP, the Cadence silicon design-in kit, and debug tools from Catalyst. “For anyone who wants to do a PCI Express design, they will know that this solution works together,” said Brad Griffin, Product Marketing Director, Allegro-SIP Product Group, Cadence Design Systems at Cadence.

Synopsys seeks to provide a one-stop shopping experience for PCI Express with their comprehensive DesignWare solution, which includes digital IP cores, PHY, and verification IP. “The Synopsys solution eases the transition to PCI Express,” said Scott Knowlton, Group Marketing Manager for the PCI product family at Synopsys. “Our IP helps customers come up to speed much more quickly. Our solution is pre-verified, through compliance, allowing customers to focus on their system-level issues.”

Mentor Graphics offers PCI Express IP solutions for both ASIC and FPGA design, as well as specialized tools for designers wanting to move their PCI Express FPGA onto a high-speed board. Their I/O Designer product allows the FPGA and PCB designer to collaborate and achieve timing closure on both the FPGA and PCB.

The promise that comes with PCI Express is exciting. Here's hoping it keeps up the PCI family tradition of performance, reliability, and longevity.

Amy Malagamba, FPGA and Programmable Logic Journal

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