



Flash News Flash

Actel Unveils ProASIC3

Could this be the iPod of FPGA families? Has Actel created the happy little "chip that could" to take on the SRAM-dominated titans of the low-cost FPGA battlefield? Will ProASIC3 Development boards be proudly displayed on the desks of any development team that wants the nice, clean look and feel of a secure, single-chip, ready-at-power-up, low-power, no-hassle solution to their high-volume, middle-of-the-technological-road design problem?

Like other programmable logic vendors, Actel has noticed that cell-based ASICs are becoming an increasingly specialized solution for high-volume electronics products. Only the best-funded, most risk-immune, highest-volume-and-performance applications can realistically justify the creation of a cell-based ASIC solution for a new product development effort. There is a growing mainstream of systems companies that are turning to FPGA and structured-ASIC solutions, even at very high production volumes. The enormity of this opportunity has brought Xilinx, Altera, Lattice, and now Actel into fierce competition for this emerging market.

Of the announcements in this value-based FPGA space over the past year, Actel's is certainly the most unique. Actel has clearly pulled out the stops on this family, leveraging their expertise and experience in flash-based FPGA design to greatest advantage. Actel claims that ProASIC3 wins in almost every category including device cost, total-system cost, performance, and power, when compared to low-cost FPGA families currently on the market. In addition, it brings along a host of additional advantages as a result of its flash-based implementation.

First, let's talk about the technical goodies. ProASIC3 is Actel's third-generation flash-based FPGA family. Unlike conventional SRAM-based FPGAs, it is designed around a fine-grained architecture (no 4-input look up tables here), which gives it a more ASIC-like behavior in layout and timing predictability. The two new families ProASIC3 and ProASIC3E range in density

from 30K to 3 million "system gates," with up to 604 user I/Os and up to 504K bits of dual-port on-chip SRAM. Actel claims up to 350MHz of "external system performance" which, even after de-rating for marketing enthusiasm, should be more than adequate for the majority of low-cost, high-volume applications.



Image courtesy of Actel Corporation.

ProASIC3's core operates at 1.5V, while I/O voltages are bank-selectable with up to 8 banks per chip and choices of 1.5V, 1.8V, 2.5V and 3.3V. For hooking up to the plethora of PCI-powered products, ProASIC3 supports 3.3V, 66MHz PCI. Power consumption is miserly compared with similar density SRAM devices, particularly in static (quiescent) power where SRAM-configuration circuitry is notoriously power-thirsty.

Actel makes a compelling argument in favor of flash as a solution for low-cost, high-volume applications. The advantages they point out are increased security, reduced power consumption, reduced device count/board area, simplified startup design, and lower power consumption. If you're worried about neutrons nailing your new digital design, Actel's flash-based logic is also immune to single-event upsets affecting the configuration logic. Also, because flash-based programmable logic is live at power-up, no boot prom or other configuration circuitry is required. This keeps the chip count down to one, reducing board area and overall system complexity.

Security is an increasing concern for many developers of high-volume applications, even those in consumer electronics who suffer profit erosion from overbuilding and cloning. ProASIC3 closes the possible SRAM-FPGA security hole of hijacking the bitstream during device configuration, eliminating the need for a backup battery at the same time. While current SRAM-based devices can also leverage encryption technologies for security, Actel's flash implementation combined with encrypted programming protocols provides a clean solution to security concerns.

Of the three "P"s (price, performance, and power) that form the traditional basis for comparing FPGA families, value-based families lean most heavily on the first. Everyone developing a solution for this market is playing the statistics, looking for the "sweet spot" that will cover the performance and power needs of 80-90% of the applications while delivering the absolute lowest possible unit and system cost.

In looking at ProASIC3's answer to the cost question, we are once again visited by our old friend, 250K unit volume with delayed availability.. While it's never fair to compare families currently shipping in volume to freshly announced future pricing, the prices we're talking here are shocking in FPGA terms. Financial analysts accustomed to the old-school dynamics of the FPGA market will need to re-adjust their spreadsheets and format the decimal over a few places to even begin to understand the realities of this emerging market segment. Think of it this way: the cheapest member of the ProASIC3 family costs less than any espresso drink at Starbuck's. The most expensive device (in volume) is still about the price of two café mochas and a poppy seed muffin.

Why is the super-low cost significant? First, it means the sales and distribution model must be fundamentally different from high-end FPGA families of the past. A 250K-unit socket win would have been a career maker for a sales rep pushing programmable devices with 4-digit price tags. With the \$1.50 (USD) starting price of ProASIC3, however, a 250K-units order is not only far from absurd, it wouldn't even dent the quota of most silicon sales sharks. Every FPGA vendor is having to re-think the ways they attract and service customers at these unit price levels. The deals may be even larger than before, but the price and volume curves are significantly changed.

The second implication of single-digit unit prices is that the cost of the device itself fades into insignificance in comparison with the rest of the surrounding system. While \$3 worth of SRAM configuration circuitry was insignificant next to a \$300 FPGA, it becomes monumental when attached to a two-dollar chip. For those of us familiar with the former situation, we'll have to look closely at the economics of our products, as the FPGA itself may no longer be the cost driver, even in an FPGA-centric product.

While we have no concrete means of evaluating any vendor's performance claims, Actel says that, in their suite of performance benchmarks, ProASIC3 averages faster speeds than competing SRAM low-cost families. This is impressive, given the common perception that flash is at a performance disadvantage in the FPGA race. Because every vendor states and evaluates

datasheet performance differently, the best way to make sure that any FPGA family will meet your performance goals is to grab one of their ridiculously inexpensive development kits and take it for a test drive with your design.

Power data is notoriously hard to translate into something meaningful for your application, but ProASIC3 should fare very well in this category, with a significant advantage over SRAM-based devices in static power consumption and at least on par with competitive families in dynamic power. The lack of startup configuration helps again here, as there is no resulting power spike at startup.

In the "more nifty features" category, Actel has incorporated a novel 1024-bit user Flash ROM (FROM) into ProASIC3. Right off the bat, they've listed a slew of possible applications for this non-volatile piece of scratch paper, including serial numbers, enabling of subscription models, crypto keys, and preference storage. Our hunch is that the design community will find as many more that Actel never considered. Given the increasingly connected nature of today's consumer applications, this seems a very clever piece of IP to have embedded.

Actel is launching ProASIC3 with complete tool and IP support. They have a wide selection of their own and third-party IP available to jumpstart your design project. They also have continued their tool strategy of offering top-notch EDA-company-supplied tools instead of an extensive internally developed suite. This means they have support now from vendors like Synplicity, Magma, Mentor Graphics, First Silicon Solutions and others.

ProASIC3 is sampling now and is slated for production-quantity delivery in Q4 of this year. This means if you operate on a normal development schedule, you can probably start designing soon and have production volumes available when you're ready. If you're one of the many teams migrating from cell-based ASIC to these new value-based FPGA technologies, that schedule alone should be music to your ears.

Kevin Morris, FPGA and Programmable Logic Journal

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